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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,910	03/20/2000	Sitaram Yadavalli	2207/7896	6697

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EXAMINER	
DAY, HERNG DER	
ART UNIT	PAPER NUMBER
2123	4

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,910	YADAVALLI ET AL.	
	Examiner	Art Unit	
	Herng-der Day	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 March 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-21 have been examined and claims 1-21 have been rejected.

Drawings

2. The drawings are objected to for the following reasons. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2-1. The Draftsperson has objected to the drawings; see the copy of Form PTO 948 for an explanation.

2-2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

(a) model sequential circuit 29, as described in line 17 of page 7.

2-3. It appears that "AND gate 20", as shown in Fig. 3A, should be "AND gate 10".

Specification

3. The disclosure is objected to because of the following informalities:

Appropriate correction is required.

3-1. It appears that "OR gate 22", as described in pages 2-3, should be "OR gate 6".

Claim Objections

4. A series of singular dependent claims is permissible in which a dependent claim refers to a preceding claim which, in turn, refers to another preceding claim.

A claim, which depends on a dependent claim, should not be separated by any claim, which does not also depend on said dependent claim. It should be kept in mind that a dependent claim may refer to any preceding independent claim. In general, applicant's sequence will not be changed. See MPEP § 608.01(n).

For example, claim 6 depends on the dependent claim 4, should not be separated by claim 5, which does not also depend on dependent claim 4.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 18 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6-1. Claim 18 depends on the dependent claim 17. However, claim 18 recites the limitation "the input signal is supplied by a user", which destroys the limitation recited in claim 17 of "the input signal is supplied by a test pattern generation system". For the purpose of claim examination, the Examiner will presume that claim 18 depends on the dependent claim 16.

6-2. Claim 20 is rejected as being dependent on the rejected claim 18.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S:C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-2, 7-9, 14-16, and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Selvidge et al., U.S. Patent 5,649,176 issued July 15, 1997.

8-1. Regarding claim 1, Selvidge et al. disclose a netlist model of a physical circuit (logic netlist, column 20, lines 8-13) comprising:

a virtual delay element, wherein said virtual delay element is coupled to a circuit element in said physical circuit (flip-flop 1602, FIG. 16B; and column 18, lines 58-63).

8-2. Regarding claim 2, Selvidge et al. further disclose an input signal is supplied to the virtual delay element (virtual clock VClk, FIG. 16B; and column 18, lines 58-63).

8-3. Regarding claim 7, Selvidge et al. further disclose the virtual delay element is one of a flip-flop or a latch (flip-flop 1602, FIG. 16B; and column 18, lines 58-63).

8-4. Regarding claim 8, Selvidge et al. disclose a method for generating a model for a physical circuit comprising:

generating a netlist model for said physical circuit (logic netlist, column 20, lines 8-13); and

providing a virtual delay element to said netlist model, wherein said virtual delay element is coupled to a physical circuit element (flip-flop 1602, FIG. 16B; and column 18, lines 58-63).

8-5. Regarding claim 9, Selvidge et al. further disclose comprising providing an input signal for said virtual delay element (virtual clock VClk, FIG. 16B; and column 18, lines 58-63).

8-6. Regarding claim 14, Selvidge et al. further disclose the virtual delay element is one of a flip-flop or a latch (flip-flop 1602, FIG. 16B; and column 18, lines 58-63).

8-7. Regarding claims 15, 16, and 21, these set of instructions claims include identical method limitations as in claims 8, 9, and 14 and are anticipated using the same analysis of claims 8, 9, and 14.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 3-6, 10-13, and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Selvidge et al., U.S. Patent 5,649,176 issued July 15, 1997, in view of Knapp et al., U.S. Patent 6,370,493 issued April 9, 2002, and filed September 10, 1998.

10-1. Regarding claims 3-6, Selvidge et al. disclose a netlist model of a physical circuit (logic netlist, column 20, lines 8-13). Selvidge et al. fails to expressly disclose: (1) the input signal is supplied by a test pattern generator or a user, and (2) the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

Knapp et al. disclose a simulation format creation system (formatting program, Knapp, column 2, lines 9-57). After verification, if the simulation result are not correct, the designer

repeatedly modifies the design, the input stimulus, and/or the expected results until the simulation results satisfy the expected results, "at which point the process proceeds to a test pattern generator module 210, which produces a series of test patterns 212 for use in testing the operation of the designed chip" (Knapp, column 5, lines 27-40). Specifically, Knapp et al. disclose the missing limitations:

(Claim 3) the input signal is supplied by a test pattern generator (inherent if the process proceeds to test pattern generator module 210 directly).

(Claim 4) the input signal is supplied by a user (the designer, Knapp, column 5, lines 31-40).

(Claims 5 and 6) the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit (test pattern generator module 210 and test patterns 212, FIG. 2; Knapp, column 5, lines 27-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Selvidge et al. to incorporate the teachings of Knapp et al. to obtain the invention as specified in claims 3-6 because the netlist model provided by Selvidge et al. is the design representation, which is an input required by the program of Knapp et al., as shown in FIG. 2.

10-2. Regarding claims 10-13, Selvidge et al. disclose a netlist model of a physical circuit (logic netlist, column 20, lines 8-13). Selvidge et al. fails to expressly disclose: (1) the input signal is supplied by a test pattern generator or a user, and (2) the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit.

Knapp et al. disclose a simulation format creation system (formatting program, Knapp, column 2, lines 9-57). After verification, if the simulation result are not correct, the designer repeatedly modifies the design, the input stimulus, and/or the expected results until the simulation results satisfy the expected results, "at which point the process proceeds to a test pattern generator module 210, which produces a series of test patterns 212 for use in testing the operation of the designed chip" (Knapp, column 5, lines 27-40). Specifically, Knapp et al. disclose the missing limitations:

(Claim 10) the input signal is supplied by a test pattern generation system (inherent if the process proceeds to test pattern generator module 210 directly).

(Claim 11) the input signal is supplied by a user (the designer, Knapp, column 5, lines 31-40).

(Claims 12 and 13) the netlist model is used by a test pattern generator to generate a test pattern for the physical circuit (test pattern generator module 210 and test patterns 212, FIG. 2; Knapp, column 5, lines 27-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Selvidge et al. to incorporate the teachings of Knapp et al. to obtain the invention as specified in claims 10-13 because the netlist model provided by Selvidge et al. is a design representation, which is an input required by the program of Knapp et al., as shown in FIG. 2.

10-3. Regarding claims 17-20, these set of instructions claims include identical method limitations as in claims 10-13 and are unpatentable using the same analysis of claims 10-13.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference to Dupenloup, U.S. Patent 6,295,636 issued September 25, 2001, and filed February 20, 1998, is cited as disclosing a RTL analysis for improved logic synthesis.

Reference to Bryant, "Extraction of Gate Level Models from Transistor Circuits by Four-Valued Symbolic Analysis", ICCAD-91, Digest of Technical Papers, 1991 IEEE International Conference on Computer-Aided Design, November 1991, pages 350-353, is cited as disclosing TRANALYZE automatically inserts unit delays on some of the transistors.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
July 14, 2003

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER